REMARKS

Claims 78-81 are added. Claims 51-53 and 55-81 are pending in the application for consideration.

Claims 51, 53, 55-56, 58-62, 64-68, 73-77 stand rejected under 35 USC §102(e) as being anticipated by Gardner et al. (U.S. Patent No. 5,923,949). Claims 52, 57, 63, 69, 70-72 stand rejected under 35 USC § 103(a) as being unpatentable over Gardner et al.

Independent claim 51 recites forming a gate oxide layer over a semiconductor substrate and providing fluorine within the gate oxide layer. Claim 51 further recites forming a gate proximate the gate oxide layer having fluoride therein after the providing. The Examiner is respectfully reminded that the PTO and Federal Circuit provide that §102 anticipation requires that **each and every element** of the claimed invention be disclosed in a single prior art reference. *In re Spada*, 911 F.2nd 705, 15 USPQ2d 1655 (Fed. Cir. 1990). The corollary of this rule is that the absence from a cited §102 reference of **any** claimed element negates the anticipation. *Kloster Speedsteel AB, et al. v. Crucible, Inc. et al.* 793 F.2d 1565, 230 USPQ 81 (Fed. Cir. 1986). Gardner does not teach, suggest, nor disclose forming a gate proximate the gate oxide layer having the fluoride therein **after the providing** the fluorine within the gate oxide layer.

Gardner teaches providing a gate (203, 303) **before** providing any fluorine in a spacer layer (207, 307) (Figs. 2A-2B and Figs. 3A-3B; Column 3, lines 10-40 and Column 4, lines 35-60). In fact, the entire disclosure of Gardner is presented to teach forming fluorine bearing sidewall spacers laterally adjacent

gate electrodes (Abstract; Column 2, lines 25-45). Logically, the gate electrodes are formed **before** the sidewall spacers are formed laterally adjacent the gate electrodes. Since the single reference Gardner does not teach or suggest all the recited elements of claim 51 as required for an appropriate §102 rejection, the rejection fails. Applicant respectfully requests allowance of claim 51 in the next Office Action.

Furthermore, the Examiner relies on the statement that it is inherent from the invention of Gardner that fluoride diffuses in the edges of the gate oxide but not in the center of the gate oxide region due to annealing (Paper No. 18, pg. 2). The Examiner's reliance on inherency is misplaced. For a teaching not presented in a reference to be inherent, the teaching must naturally follow from the teachings actually presented in the reference. The purpose of providing fluorine in sidewall spacers as taught by Gardner is to reduce the susceptability of the resultant semiconductor device to hot carrier injection of electrons into the gate electrode and/or gate oxide (Background of the Invention; Column 3, lines 25-30). However, Gardner specifically states that providing fluoride into the gate oxide or gate oxide/silicon interface does not prevent hot carrier injection from persisting. (Column 2, lines 15-25). Clearly, Gardner teaches away from providing fluoride in a gate oxide. Accordingly, no reasonable argument can be made that from the teachings of Gardner, it naturally follows that fluorine is diffused into the gate oxide. The Examiner's inherency argument must fail. At a minimum, the Examiner's inherency argument is negated because Gardner states fluorine in the gate oxide does not prevent hot carrier effects, and

accordingly, provides no teachings of fluorine diffusing into the gate oxide layer. For at least these reasons, the Examiner's inherency arguments must fail, and correspondingly, the rejection against claim 51 must fail. Claim 51 is allowable.

Furthermore, the Examiner's inherency argument relies on the assumption that the annealing temperature is high enough to diffuse fluorine from the sidewall spacers into the gate oxide. This assumption simply can not be made. A typical annealing temperature is below a typical diffusion temperature. Referring to the reference: *Microchip Fabrication*, 3rd Edition, by Peter Van Zant, Doping, Chapter 11 (provided in an Information Disclosure Statement with this response), pages 311-349, typical annealing and diffusion temperatures are provided. A typical annealing temperature for restoration of crystal damage and electrical activation is below a typical diffusion temperature (page 343). Additionally, the reference specifically states the reasoning is to prevent lateral diffusion of a dopant (page 343). A typical anneal in a furnace will take place between 600 and 1000°C in a hydrogen atmosphere (page 343) and a typical temperature range for diffusion is provided as 1,050-1,200°C (Fig. 11.26 of page 330). Accordingly, this reference teaches, that relying on an annealing temperature as inherently providing a temperature necessary to diffuse fluorine from a sidewall spacer into a gate oxide is clearly erroneous. In fact, one contrary teaching is the antithesis of inherency. Applicant respectfully requests withdrawal of the inherency arguments, and therefore, withdrawal of the §102 rejection against Claim 51. For at least these reasons, Claim 51 is allowable.

Claims 52-53 and 76-77 depend from independent claim 51, and therefore are allowable for the reasons discussed above with respect to the independent claim, and for their own recited features which are neither shown or taught by the cited art.

Claim 55 recites forming a gate and a gate oxide layer in overlapping relation and concentrating at least one of chlorine or fluorine in the gate oxide layer. In rejecting Claim 55, the Examiner relies on the inherency argument. However, it does not follow from the teachings of Gardner that fluorine diffuses into the gate oxide due to annealing. Gardner clearly teaches that fluorine provided in a gate oxide does not prevent hot carrier injection, and then teaches to provide sidewall spacers having fluorine to prevent the hot carrier effect. (Column 2, lines 15-25). Accordingly, the argument that Gardner inherently teaches providing fluorine in a gate oxide has to be rejected. Furthermore, routine annealing temperatures are purposely provided at temperature ranges below temperatures that cause diffusion of dopants, and therefore, the Examiner's inherency argument is negated and must fail. For at least these reasons, Claim 55 is allowable, and applicant expects allowance of Claim 55 in the next Office Action.

Claims 56-61 depend from independent Claim 55, and therefore, are allowable for the reasons discussed above with respect to the independent claim, and for their own recited features which are neither shown nor taught by the cited art.

Claim 62 recites forming a gate and gate oxide layer in overlapping relation, and doping the gate oxide layer within the overlap with at least one of chlorine or fluorine. In rejecting Claim 62, the Examiner relies on the inherency argument. However, it does not follow from the teachings of Gardner that fluorine diffuses into the gate oxide due to annealing. Gardner clearly teaches that fluorine provided in a gate oxide does not prevent hot carrier injection, and then teaches to provide sidewall spacers having fluorine to prevent the hot carrier effect. (Column 2, lines 15-25). Accordingly, the argument that Gardner inherently teaches providing fluorine in a gate oxide has to be rejected. Furthermore, routine annealing temperatures are purposely provided at temperature ranges below temperatures that cause diffusion of dopants, and therefore, the Examiner's inherency argument is negated and must fail. For at least these reasons, Claim 62 is allowable, and applicant expects allowance of Claim 62 in the next Office Action.

Claims 63-67 depend from independent Claim 62, and therefore, are allowable for the reasons discussed above with respect to the independent claim, and for their own recited features which are neither shown nor taught by the cited art.

Claim 68 recites forming a gate over a gate oxide layer and diffusing doping at least one of chlorine or fluorine into the gate oxide layer beneath the gate. In rejecting Claim 68, the Examiner relies on the inherency argument. However, it does not follow from the teachings of Gardner that fluorine diffuses into the gate oxide due to annealing. Gardner clearly teaches that fluorine

provided in a gate oxide does not prevent hot carrier injection, and then teaches to provide sidewall spacers having fluorine to prevent the hot carrier effect. (Column 2, lines 15-25). Accordingly, the argument that Gardner inherently teaches providing fluorine in a gate oxide has to be rejected. Furthermore, routine annealing temperatures are purposely provided at temperature ranges below temperatures that cause diffusion of dopants, and therefore, the Examiner's inherency argument is negated and must fail. For at least these reasons, Claim 68 is allowable, and applicant expects allowance of Claim 68 in the next Office Action.

Claims 69-75 depend from independent Claim 68, and therefore, are allowable for the reasons discussed above with respect to the independent claim, and for their own recited features which are neither shown nor taught by the cited art.

Since all the independent claims are rejected under §102 in which the Examiner relies on the inherency argument, all the claims, including the dependent claims, are rejected relying on the inherency argument. However, the inherency argument is improper for at least the reasons set forth above. If any of the claims are not found allowable, then pursuant to §2144.03 of the M.P.E.P., applicant hereby requests identification of prior art which discloses the features not found in this single reference and which is properly combinable with the reference, or an affidavit in support of the rejections.

This application is now believed to be in immediate condition for allowance, and action to that end is respectfully requested. If the Examiner's next

anticipated action is to be anything other than a Notice of Allowance, the undersigned respectfully requests a telephone interview prior to issuance of any such subsequent action.

Respectfully submitted,

Dated: 7-5-01 By: _____

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Application Serial No. 09/292,132
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Inventor ..... Salman Akram et al.
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Group Art Unit 2812
Examiner ..... S. Mulpuri
Attorney's Docket No. MI22-1171
Title: Methods of Forming a Transistor Gate

VERSION WITH MARKINGS TO SHOW CHANGES MADE ACCOMPANYING RESPONSE TO APRIL 5, 2001 OFFICE ACTION

In the Claims

The claims have been amended as follows. Underlines indicate insertions and ~~strikeouts~~ indicate deletions.

78. The method of claim 51 wherein the providing the fluorine within the gate oxide layer provides a concentration of fluorine effective to diminish hot carrier effects.

79. The method of claim 55 wherein the concentrating the at least one of chlorine or fluorine provides a concentration of chlorine or fluorine effective to diminish hot carrier effects.

80. The method of claim 62 wherein the doping the gate oxide layer with the at least one of chlorine or fluorine provides a concentration of chlorine or fluorine effective to diminish hot carrier effects.

81. The method of claim 68 wherein the diffusion doping the at least one of chlorine or fluorine into the gate oxide layer provides a concentration of chlorine or fluorine effective to diminish hot carrier effects.

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